Amendment to the Specification:

Please replace the Abstract with the following:

ABSTRACT

~~Disclosed is a~~ A matched filter for implementing the correlation of an input signal and a reference signal. The matched filter comprises N parallel M-sample long shift registers for receiving an equal number of input signals at the sampling frequency of the input signal, wherein $N \geqslant 2$. The matched filter also stores K reference signals, wherein $K \geqslant 2$, and then multiplexes one of the input signals and one of the reference signals at a time to calculation logic by applying alternately at least one combination of the input signals and the reference signals to the calculation logic. The calculation logic may then calculate the correlation time-dividedly for each combination of an input signal and a reference signal so that correlation results calculated from different signals appear at the output of the calculation means as a sequence.

Please replace the paragraph beginning on page 11, line 21 with the following:

The reference signal applied at each particular time from the reference shift register (or reference memory) 6-26 and from the data shift register 6-22, and the I and Q signals are multiplied by each other in a multiplier block 6-31. If both signals are composed of 1-bit samples, the multiplication may be carried

out for example with an XNOR gate whose output is 1 if its two inputs are equal. In another embodiment, the multiplication may be carried out with an XOR circuit. After this multiplication, there are N_{MF} data values 6-28.